SiP Global Summit Day 1

Theme: Wafer Level System Integration for Edge Computing, HPC and AI

THURSDAY, SEPTEMBER 06

8:00am	**Registration**
8:30am	**Opening Remarks by SEMI Executives**
	Mr. Tom Salmon, Vice President, Collaborative Technology Platforms / Executive Director, FOA, SEMI
8:35am	**Welcome Remarks & Moderator**
	Dr. Kuo-Chung Yee/ 余國寵, Director, TSMC
8:50am	**Keynote 1: Synergistic Growth of AI and Silicon Age 4.0 through Heterogeneous Integration of Technologies**
	Dr. Nicky Lu/ 盧超群, CEO, Chairman and Founder, Etron
9:30am	**Keynote 2: Product Applications and Technology Requirements of System in Package**
	Mr. HW Kao/ 高學武, Corporate Vice President, MediaTek
10:10am	**Keynote 3: Advanced System Integration Technology Trends**
	Dr. Douglas Yu/ 余振華, Vice President, Research & Development / Integrated Interconnect & Packaging, TSMC
10:50am	**Break**
11:00am	**Topic 1: Enabling Designs beyond Moore - Wafer Level Integration**
	Mr. Saugat Sen, Vice President, R&D, Cadence
11:30am	**Topic 2: HBM Trends and Market Outlook**
	Dr. DY Shim, Vice President , Head of HBM Business, SK Hynix
12:00pm	**Lunch Break**
1:00pm	**Topic 3: Advanced Packaging for High-end Applications**
	Mr. Jérôme AZEMAR, Director, Yole Développement
1:30pm	**Topic 4: InFO_AIP Technology for 5G Applications**
	Dr. Chuei-Tang Wang/ 王垂堂, Director, TSMC
2:00pm	**Topic 5: Silicon Photonics Technology driving the Datacenter Interconnect Roadmap**
	Dr. Peter De Dobbelaere, Vice Presidnet of Engineering, Luxtera
2:30pm	**Topic 6: Challenges for Exa-scale Data Center Optical Interconnect**
	Dr. Andy Knights, Lead Silicon Architect, Ranovus
3:00pm	**Break**
3:15pm	**Topic 7: Opportunities and Challenges of Advanced Wafer Level Packages Applied in Heterogeneous Integration Devices**
	Mr. Albert Lan/藍章益 , Global Packaging TD, Applied Materials
3:45pm	**Topic 8: Chemistry Solutions for Enhanced Reliability of Sub 5 μm L/S RDL for 5G**
	Dr. Ralf Schmidt, R&D Team Manager, Atotech
4:15pm	**Topic 9: Customization Service: A Collaboration Model to Effectively Develop Production Worthiness Process Equipment for the Back-end Wafer Level Packaging Industry**
	Mr. Michael Lay/ 賴炫宇 , President, Leading Precision Inc.
4:45pm	**Lucky Draw by SPIL**
4:50pm	**Adjournment**